

MULTIPLEXING APPARATUS

BACKGROUND OF THE INVENTION

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The present invention relates to a multiplexing
5 apparatus which multiplexes data items received from
lines on plural terminal sides to transmit the
multiplexed data onto a line on a network side, and
demultiplexes the multiplexed data received from the
line on the network side to transmit the demultiplexed
10 data items onto the lines on the plural terminal sides.

A constitution of a conventional multiplexing
apparatus is shown in Fig. 5.

In Fig. 5, reference numerals 21 to 23 denote
terminal interface units. Here, the terminal
15 interface unit 21 is a voice line interface unit which
accommodates a PBX (Private Branch Exchange) 5
accommodating voice terminals such as a telephone 6.
The terminal interface unit 22 is a data line interface
unit for accommodating a data terminal 4. The terminal
20 interface unit 23 is an FR (Frame Relay) line interface
unit for accommodating an FR terminal 3. Furthermore,
reference numeral 24 denotes a network interface unit
for accommodating a line on a network 1 side.

The terminal interface units 21 to 23 and the
25 network interface unit 24 are connected to each other
by an internal bus 26, and data is sent/received

therebetween via the internal bus 26. Furthermore, reference numeral 25 denotes an internal bus control unit which arbitrates the bus right among devices connected to the internal bus 26.

5 In the terminal interface units 21 to 23, data transmitted from the terminal is received by the terminal-side line interface sub-unit 211, and then converted to a data block (hereinafter generically called packet type data) as a certain unit, to which
10 a destination is given, by an assembly/disassembly sub-unit 28. The data block is an ATM cell, an IP packet and the like, and determined by a protocol adopted in the network 1. The data block is transmitted to the internal bus 26 from an internal bus interface sub-unit
15 271. Furthermore, in the terminal interface units 21 to 23, packet type data transmitted from the network interface unit 24 via the internal bus 26 is received by the internal bus interface sub-unit 271 and then disassembled by the assembly/disassembly sub-unit 28,
20 and data is extracted. The extracted data is transmitted from the terminal-side line interface sub-unit 211 to the terminal.

On the other hand, in the network interface unit 24, the packet type data transmitted from each of the
25 terminal interface units 21 to 23 via the internal bus 26 is received by an internal bus interface sub-unit

272, and then sent to a priority control sub-unit 242 via a network synchronizing sub-unit 241. The packet type data is once stored in a priority control buffer 243. Thereafter, packet type data is sequentially
5 synchronized with the line on the network 1 side in the order of descending priorities, the priority being stored in a header of the packet type data, by the network synchronizing sub-unit 241 to be transmitted to the line on the network 1 side. Furthermore, in the network
10 interface unit 24, the packet type data transmitted from the line on the network 1 side is received by the network synchronization sub-unit 241, and then transmitted from the internal bus interface sub-unit 272 to the internal bus 26 to be received by each of
15 the terminal interface units 21 to 23 as described above.

Furthermore, in the network interface unit 24, a clock extraction sub-unit 244 extracts a network clock synchronized with the line on the network 1 side, and sends the extracted network clock to the internal bus
20 control unit 25. From this network clock, a clock generation sub-unit 251 of the internal bus control unit 25 generates operation clocks for the internal bus 26 and the terminal interface units 21 to 23, and distributes the operation clocks to the internal bus
25 26 and the terminal interface units 21 to 23.

SUMMARY OF THE INVENTION

The conventional multiplexing apparatus adopts the constitution to perform the sending/receiving of the packet type data between the terminal interface units 21 to 23 and the network interface unit 24 via the internal bus 26 as described above. Therefore, the internal bus interface sub-units 271 and 272 must be provided in the terminal interface units 21 to 23 and the network interface unit 24, respectively.

Furthermore, the internal bus control unit 25 for arbitrating the bus rights among the devices connected to the internal bus 26 must be provided. These units are a factor to upsize the circuit of the multiplexing apparatus.

The present invention has been made with above problems taken into consideration, and has its object to enable the size of the circuit of the multiplexing apparatus to be reduced.

To achieve the foregoing object, the multiplexing apparatus of the present invention comprises a plurality of terminal interface units respectively accommodating lines on terminal sides; a buffer unit which is connected to each of the terminal interface units by the point-to-point connection; and a network interface unit connected to the buffer unit, the network interface unit accommodating a line on a network side.

Each of the terminal interface units converts data received from the line on the terminal side to packet type data, and transmits the packet type data to the buffer unit via a corresponding point-to-point connection line. Each of the terminal interface units disassembles packet type data received from the buffer unit via the corresponding point-to-point connection line, and extracts data therefrom to transmit the extracted data to the corresponding line on the terminal side.

The buffer unit includes a packet type data storing unit for storing the packet type data received from a plurality of the terminal interface units. The buffer unit reads out the packet type data sequentially from the packet type data storing unit, and transmits the packet type data to the network interface unit. The buffer unit receives packet type data transmitted from the network interface unit, and selects a terminal interface unit in accordance with a destination of the packet type data received. The buffer unit transmits this packet type data to the selected terminal interface unit via the corresponding point-to-point connection line.

The network interface unit receives the packet type data transmitted from the buffer unit, and synchronizes the packet type data with the line on the

network side to transmit the packet type data to the line on the network side. Furthermore, the network interface unit receives packet type data transmitted from the line on the network side, and transmits this
5 packet type data to the buffer unit.

According to the present invention, since an internal bus which is necessary for the bus arbitration is not used in the above constitution, the internal bus interface sub-units 271 of the terminal interface
10 units 21 to 23 and the internal bus interface sub-unit 272 of the network interface unit 24 as well as the internal bus control unit 25 for arbitrating the bus right among the devices connected to the internal bus 26, which are shown in Fig. 5, are unnecessary. Thus,
15 it is possible to facilitate downsizing of the circuit size of the multiplexing apparatus.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a constitution
20 of a communication system using an ATM multiplexing apparatus to which a first embodiment of the present invention is applied.

Fig. 2 is a block diagram showing a constitution of the ATM multiplexing apparatus shown in Fig. 1.

25 Fig. 3 is a block diagram showing a constitution of a communication system using an IP multiplexing

apparatus to which a second embodiment of the present invention is applied.

Fig. 4 is a block diagram showing a constitution of the IP multiplexing apparatus shown in Fig. 3.

5 Fig. 5 is a block diagram showing a constitution of a conventional multiplexing apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be
10 described below.

At first, a first embodiment of the present invention will be described.

In Fig. 1, shown is a constitution of a communication system using an ATM (Asynchronous
15 Transfer Mode) multiplexing apparatus to which the first embodiment of the present invention is applied.

In Fig. 1, reference numeral 1a denotes an ATM network; 3 denotes an FR terminal; 4 denotes a data terminal; 5 denotes a PBX; 6 denotes a voice terminal
20 such as a telephone; and 2a denotes the ATM multiplexing apparatus to which the first embodiment of the present invention is applied.

In such a constitution, the ATM multiplexing apparatus 2a multiplexes data items received from the
25 FR terminal 3, the data terminal 4 and/or the PBX 5, which are accommodated therein, and transmits the

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multiplexed data to a line on the ATM network 1a side. Furthermore, the ATM multiplexing apparatus 2a demultiplexes multiplexed data which is received from the line on the ATM network 1a side, and transmits this data items to the FR terminal 3, the data terminal 4 and/or the PBX 5. Thus, each of the FR terminal 3, the data terminal 4 and the PBX 5 accommodated in this ATM multiplexing apparatus 2a is enabled to communicate with the FR terminal 3, the data terminal 4 and/or the PBX 5 accommodated in one of other ATM multiplexing apparatuses 2a disposed so as to be opposite to this ATM multiplexing apparatus 2a via the ATM network 1a.

A constitution of the ATM multiplexing apparatus 2a shown in Fig. 1 is shown in Fig. 2.

15 In Fig. 2, reference numerals 21a to 23a denote terminal interface units. Here, the terminal interface unit 21a is a voice line interface unit for accommodating the PBX 5 in which voice terminals such as a telephone 6 are accommodated. The terminal interface unit 22a is a data line interface unit for accommodating the data terminal 4. The terminal interface unit 23a is an FR line interface unit for accommodating the FR terminal 3. Furthermore, reference numeral 24a denotes an ATM network interface unit for accommodating the line on the ATM network 1a side; 242a denotes a priority control unit comprising

a priority control buffers 243a each provided for each of the terminal interface units 21a to 23a; and 251a denotes a clock generation unit.

Here, each of the terminal interface units 21a to 23a is directly connected to the corresponding one of the priority control buffers 243a in the priority control unit 242a by the point-to-point connection, that is, without an internal bus which is necessary for the bus arbitration. Each of the priority control buffers 243a sends/receives an ATM cell directly to/from the corresponding one of the terminal interface units 21a to 23a.

In the terminal interface units 21a to 23a, data transmitted from the terminal is received by the terminal-side line interface sub-unit 211a, and then stored in the ATM cell by the cell assembly/disassembly sub-unit 28a. Then, the ATM cell is transmitted to the corresponding one of the priority control buffers 243a in the priority control unit 242a via a corresponding point-to-point connection line. Furthermore, in the terminal interface units 21a to 23a, an ATM cell transmitted from the corresponding priority control buffer 243a in the priority control unit 242a is disassembled by the corresponding one of the cell assembly/disassembly sub-unit 28a, and data is extracted therefrom. Then, the extracted data is

transmitted to the terminal from the terminal-side line interface sub-unit 211a.

Each of the priority control buffers 243a in the priority control unit 242a stores the ATM cell
5 transmitted from the corresponding one of the terminal interface sub-units 21a to 23a. The priority control unit 242a retrieves contents of each of the priority control buffers 243a, and sequentially reads out the ATM cell stored in each of the priority control buffers
10 243a in the order of descending priorities, the priority being stored in a header of each ATM cell, and transmits the ATM cell to the ATM network interface unit 24a. Furthermore, the priority control unit 242a receives an ATM cell transmitted from the ATM network interface
15 unit 24a, and selects one of the terminal interface units 21a to 23a in conformity with a destination of the ATM cell. Then, the priority control unit 242a transmits the ATM cell to the selected one of the terminal interface units 21a to 23a via the
20 corresponding point-to-point connection line.

In the ATM network interface unit 24a, the ATM cell transmitted from the priority control unit 242a is received by the network synchronizing unit 241a, and thereafter synchronized with the line of the ATM
25 network 1a to be transmitted to the line of the ATM network 1a. Moreover, in the ATM network interface unit

24a, the ATM cell transmitted from the line of the ATM network 1a is received by the network synchronizing unit 241 to be transmitted to the priority control unit 242a. In the ATM network interface unit 24a, a clock extraction sub-unit 244a extracts a network clock synchronized with the line of the ATM network 1a.

The clock generation unit 251a generates operation clocks for the priority control unit 242a and the terminal interface units 21a to 23a from the network clock extracted by the clock extraction sub-unit 244a, and distributes the operation clocks thereto.

With such a constitution, in this embodiment, the sending/receiving of the ATM cell between the priority control unit 242a and the ATM network interface unit 24a is performed in synchronization with the network clock extracted by the clock extraction sub-unit 244a, that is, at a speed equal to a transmission speed of the line of the ATM network 1a. Accordingly, it is unnecessary to provide a buffer for regulating the speed in the ATM interface unit 24a. Furthermore, the ATM multiplexing apparatus 2a of this embodiment can deal with various transmission speeds of the line of the ATM network 1a.

The speed of the sending/receiving of the ATM cell between each of the terminal interface units 21a to

23a and the priority control unit 242a may be satisfactorily a speed so that an ATM cell to be transmitted to the line of the ATM network 1a is not lost in the terminal interface units 21a to 23a and
5 data to be transmitted to each terminal is not lost in the priority control unit 242a.

The first embodiment of the present invention was described as above.

According to this embodiment, each of the terminal
10 interface units 21a to 23a is connected directly to the corresponding one of the priority control buffers 243a in the priority control unit 242a by the point-to-point connection. Specifically, the ATM multiplexing apparatus 2a of this embodiment adopts
15 the constitution in which an internal bus, which is necessary for the bus arbitration, is not used. Accordingly, it is unnecessary to provide internal bus interface units for the terminal interface units 21a to 23a and the ATM network interface unit 24a and an
20 internal bus control unit for arbitrating the bus right among the devices connected to the internal bus, which were conventionally required. Thus, it is possible to downsize a circuit of the ATM multiplexing apparatus.

Next, a second embodiment of the present invention
25 will be described.

In Fig. 3, shown is a constitution of a

communication system using an IP (Internet Protocol) multiplexing apparatus to which the second embodiment of the present invention is applied. Here, constituent components having identical functions to those of the constituent components shown in Fig. 1 are denoted by the identical reference numerals.

In Fig. 3, reference numeral 1b denotes an IP network, and reference numeral 2b denotes an IP multiplexing apparatus to which the second embodiment of the present invention is applied.

In such a constitution, the IP multiplexing apparatus 2b multiplexes data items received from the FR terminal 3, the data terminal 4 and/or the PBX 5, which are accommodated therein, and transmits the multiplexed data to a line on the IP network 1b side. The IP multiplexing apparatus 2b demultiplexes multiplexed data received from the line on the IP network 1b side, and transmits data items to the FR terminal 3, the data terminal 4 and/or the PBX 5. Thus, each of the FR terminal 3, the data terminal 4 and the PBX 5 accommodated in this IP multiplexing apparatus 2b is enabled to communicate with the FR terminal 3, the data terminal 4 and/or the PBX 5 accommodated in one of other IP multiplexing apparatuses 2b disposed so as to be opposite to this IP multiplexing apparatus 2b via the IP network 1b.

A constitution of the IP multiplexing apparatus 2b shown in Fig. 3 is shown in Fig. 4. Here, constituent components having identical functions to those of the constituent components shown in Fig. 2 are denoted by
5 the identical reference numerals.

In Fig. 4, reference numerals 21b to 23b denote terminal interface units. Here, the terminal interface unit 21b is a voice line interface unit for accommodating the PBX 5 in which voice terminals such
10 as telephones 6 are accommodated. The terminal interface unit 22b is a data line interface unit for accommodating the data terminal 4. The terminal interface unit 23b is an FR line interface unit for accommodating the FR terminal 3. Furthermore,
15 reference numeral 24b denotes an IP network interface unit for accommodating the line of the IP network 1b.

Here, each of the terminal interface units 21b to 23b is directly connected to the corresponding one of the priority control buffers 243a in the priority
20 control unit 242a by the point-to-point connection, that is, without an internal bus which is necessary for the bus arbitration. Each of the priority control buffers 243a sends/receives an IP packet directly to/from the corresponding one of the terminal interface
25 units 21b to 23b.

In the terminal interface units 21b to 23b, data

transmitted from the terminal is received by the terminal-side line interface sub-unit 211a, and then converted to the IP packet by the packet assembly/disassembly sub-unit 28b. Then, the IP packet is transmitted to the corresponding one of the priority control buffers 243a in the priority control unit 242a via a corresponding point-to-point connection line. Furthermore, in the terminal interface units 21b to 23b, an IP packet transmitted from the corresponding priority control buffer 243a in the priority control unit 242a is disassembled by the corresponding one of the packet assembly/disassembly sub-unit 28b, and data is extracted therefrom. Then, the extracted data is transmitted to the terminal from the terminal-side line interface sub-unit 211a.

Each of the priority control buffers 243a in the priority control unit 242a stores the IP packet transmitted from the corresponding one of the terminal interface sub-units 21b to 23b. The priority control unit 242a retrieves contents of each of the priority control buffers 243a, and sequentially reads out the IP packet stored in each of the priority control buffers 243a in the order of descending priorities, the priority being stored in a header of each IP packet, and transmits the IP packet to the IP packet interface unit 24b. Furthermore, the priority control unit 242a receives

an IP packet transmitted from the IP network interface unit 24b, and selects one of the terminal interface units 21b to 23b in conformity with a destination of the IP packet (IP address). Then, the priority control unit 242a transmits the IP packet to the selected one of the terminal interface units 21b to 23b via the corresponding point-to-point connection line.

In the IP network interface unit 24b, the IP packet transmitted from the priority control unit 242a is received by a network synchronizing unit 241b, and thereafter synchronized with the line of the IP network 1b to be transmitted to the line of the IP network 1b. Moreover, in the IP network interface unit 24b, the IP packet transmitted from the line of the IP network 1b is received by the network synchronizing unit 241b to be transmitted to the priority control unit 242a. In the IP network interface unit 24b, a clock extraction sub-unit 244b extracts a network clock synchronized with the line of the IP network 1b.

The clock generation unit 251a generates operation clocks for the priority control unit 242a and the terminal interface units 21b to 23b from the network clock extracted by the clock extraction sub-unit 244b, and distributes the operation clocks thereto.

With such a constitution, in this embodiment, the

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5 sending/receiving of the IP packet between the priority control unit 242a and the IP network interface unit 24b is performed in synchronization with the network clock extracted by the clock extraction sub-unit 244b, that is, at a speed equal to a transmission speed of the line of the IP network 1b. Accordingly, it is unnecessary to provide a buffer for regulating the speed in the IP interface unit 24b. Furthermore, the IP multiplexing apparatus 2b of this embodiment can deal
10 with various transmission speeds of the line of the IP network 1b.

15 The speed of the sending/receiving of the IP packet between each of the terminal interface units 21b to 23b and the priority control unit 242a may be satisfactorily a speed so that an IP packet to be transmitted to the line of the IP network 1b is not lost in the terminal interface units 21b to 23b and data to be transmitted to each terminal is not lost in the priority control unit 242a.

20 The second embodiment of the present invention was described as above.

25 In this embodiment, similarly to the foregoing first embodiment, each of the terminal interface units 21b to 23b is directly connected to the corresponding one of the priority control buffers 243a in the priority control unit 242a by the point-to-point connection.

Specifically, the IP multiplexing apparatus 2b of this embodiment adopts the constitution in which an internal bus which is necessary for the bus arbitration is not used. Accordingly, it is unnecessary to provide
5 internal bus interface units for the terminal interface units 21b to 23b and the IP network interface unit 24b and an internal bus control unit for arbitrating the bus right among the devices connected to the internal bus, which were conventionally required. Thus, it is
10 possible to downsize a circuit of the IP multiplexing apparatus.

It should be noted that the present invention is not limited to the foregoing embodiments, and various changes, substitution and alternations can be made
15 therein without departing from spirit and scope of the invention.

In the foregoing embodiments, for example, adopted is the constitution in which the priority control buffer 243a is provided for each terminal
20 interface unit, and each priority control buffer 243a is directly connected to the corresponding one of the terminal interface units by the point-to-point connection. However, the present invention is not limited to this. In the priority control unit 242a,
25 an input/output interface sub-unit may be satisfactorily provided for each terminal interface

unit. A constitution in which each input/output interface sub-unit is directly connected to the corresponding one of the terminal interface units by the point-to-point connection may be adopted. In this case, the priority control unit 242a controls writing/reading of data to/from the priority control buffer 243a, whereby the number of the priority control buffers 243a may be one.

Furthermore, the first and second embodiments were described by exemplifying the ATM multiplexing apparatus connected to the ATM network 1a and the IP multiplexing apparatus connected to the IP network 1b, respectively. However, the present invention is not limited to these. The present invention can be applied to a multiplexing apparatus which accommodates lines from a plurality of terminals, converts data transmitted from each terminal to packet type data items, and multiplexes the data items to transmit to a network.

As described above, according to the present invention, the circuit size of the multiplexing apparatus can be reduced.